What is claimed is:

1. A method for performing an erase verification operation on a non-volatile memory device having a plurality of blocks of memory each having groups of memory sub-blocks, each memory sub-block comprising a plurality of memory cells and an erase indication register, the method comprising:
loading a memory sub-block start address of a first memory sub-block having an erase indication register that indicates the first memory sub-block is not erased;
sequentially reading the plurality of memory cells of the memory sub-block;
if a first memory cell is not erased, storing an address of the first memory cell into a verification address pointer for the memory sub-block;
if the first memory cell is not erased, jumping to a second memory sub-block;
if the first memory cell is erased, sequentially reading the plurality of memory cells until either an end of the first memory sub-block occurs or a second memory cell is not erased; and
if the end of the first memory sub-block occurs with each of the plurality of memory cells erased, setting the erase indication register to indicate that the first memory sub-block is erased.

2. The method of claim 1 wherein the erase indication register is programmed during a prior erase verification operation.

3. The method of claim 1 and further including, if the first memory cell is not erased, sequentially reading memory cells of the second sub-block prior to applying the second erase pulse.

4. The method of claim 1 and further comprising loading the memory sub-block start address after performing an erase operation.

5. The method of claim 1 wherein the memory sub-block start address is stored in a register circuit.

6. A non-volatile memory device comprising:

a plurality of blocks of memory each having groups of memory sub-blocks, each memory sub-block comprising a plurality of memory cells and an erase indication register; and

control circuitry coupled to the plurality of blocks of memory, the control circuitry capable of executing an erase verification operation comprising loading a memory sub-block start address of a first memory sub-block having an erase indication register that indicates the first memory sub-block is not erased, sequentially reading the plurality of memory cells of the memory sub-block, if a first memory cell is not erased, storing an address of the first memory cell into a verification address pointer for the memory sub-block and jumping to a second memory sub-block, if the first memory cell is erased, sequentially reading the plurality of memory cells until either an end of the first memory sub-block occurs or a second memory cell is not erased, and when the end of the first memory sub-block occurs with each of the plurality of memory cells erased, setting the erase indication register to indicate that the first memory sub-block is erased.

7. The device of claim 6 wherein the control circuitry is a state machine.

8. A memory system comprising:

a processor that generates control signals; and

a non-volatile memory device coupled to the processor, the device comprising:

a plurality of blocks of memory each having groups of memory sub-blocks, each memory sub-block comprising a plurality of memory cells and an erase indication register; and

control circuitry coupled to the plurality of blocks of memory, the control circuitry capable of executing an erase verification operation in response to the processor control signals, the operation comprising loading a memory sub-block

start address of a first memory sub-block having an erase indication register that indicates the first memory sub-block is not erased, sequentially reading the plurality of memory cells of the memory sub-block, if a first memory cell is not erased, storing an address of the first memory cell into a verification address pointer for the memory sub-block and jumping to a second memory sub-block, if the first memory cell is erased, sequentially reading the plurality of memory cells until either an end of the first memory sub-block occurs or a second memory cell is not erased, and when the end of the first memory sub-block occurs with each of the plurality of memory cells erased, setting the erase indication register to indicate that the first memory sub-block is erased.